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RN-6789

B. E. III (Sem. V) (ECC) Examination

May / June – 2010

Digital Microelectrics & Circuits : Paper - II

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 5) (ECC)**

Name of the Subject :

☛ **Digital Microelectrics & Circuits - 2**

☛Subject Code No. : **6 7 8 9** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data whenever necessary.

SECTION - I

1 (a) Do as directed : **10**

(i) Explain fan in.
(ii) Explain one merit and demerit of ECL logic family.
(iii) Temperature sensitivity of HTL is lower than DTL state true or false.
(iv) DTL is faster than TTL. State true or false.
(v) Explain passive pull up.
(vi) What is the basic function realized in RTL logic family?
(vii) What output state determines the fanout in TTL gate.
(viii) State the disadvantages of DCTL logic family.
(ix) Draw the internal structure of lateral transistor.
(x) ECL family is also called as _____ family.

(b) (i) Explain propagation time and propagation delay hazards. **5**

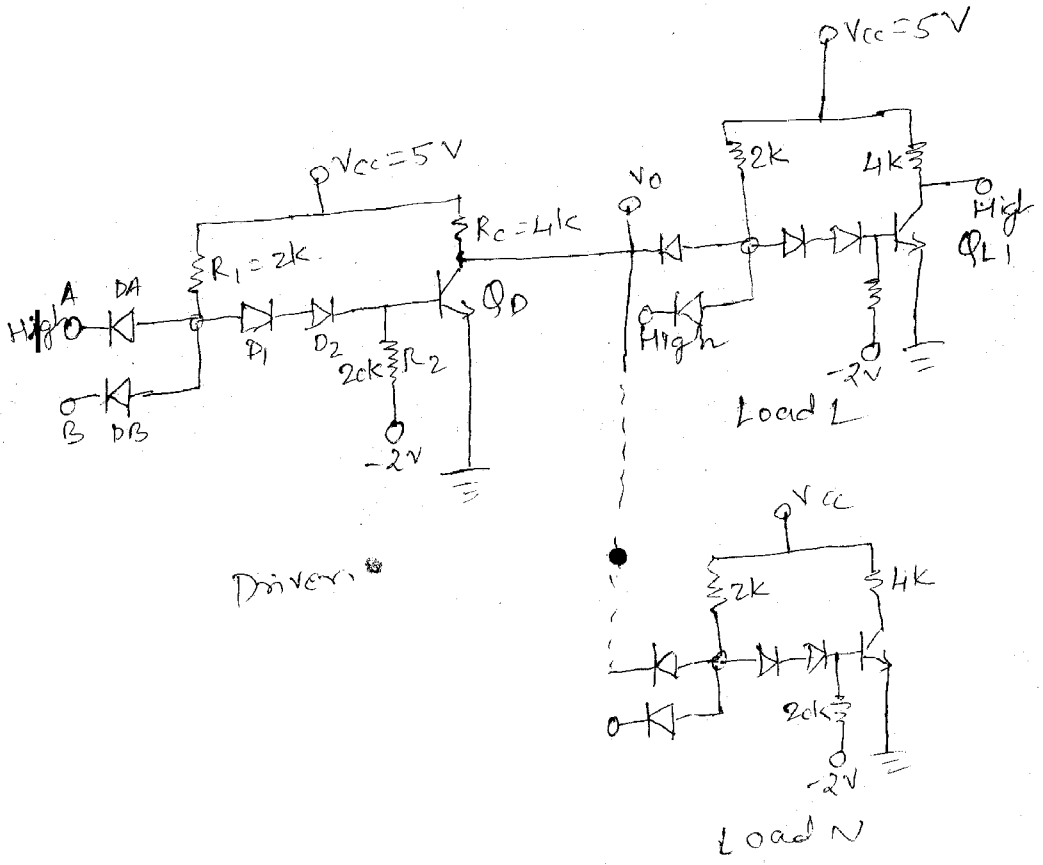
(ii) Draw internal construction of multi emitter transistor and explain basic gate with multi emitter transistor. **5**

2 (a) Draw and explain transfer characteristics of a standard TTL NAND gate. 8

(b) Explain discrete DTL NAND gate. 7

OR

2 (a) Determine the logic low fanout of the DTL gate shown in the figure below. Assume β of 50 for all transistors. 7



(b) Explain advantages of negative power supply in ECL. 8

3 Attempt any three : 15

(i) Explain RTL exclusive OR gate.

(ii) Explain physical layout of IIL.

(iii) Explain high threshold DTL gate

(iv) State atleast one merit and demerit of following logic family :
I^2L, DCTL, TTL, RTL.

SECTION - II

4 (a) Write answers in short preferably in few words : **7**

(i) State any **two** characteristic of DRAM.

(ii) What types of memories are nonvolatile?

(iii) Name any **two** manufacture of CPLD.

(iv) In CMOS logic family how many transistors are required to implement Boolean function $Y = \overline{A + BC}$?

(v) How is given unit of data located in memory?

(vi) List types of read-only memories.

(vii) In dynamic shift register, maximum frequency of operation depends on charge transfer rate. True or False? If statement is false, make necessary correction.

(b) Fill in the blanks : (each blank carry one mark) **7**

(i) In CMOS NAND gate driver transistors are connected in _____ and load transistors are connected in _____.

(ii) $PMOS_{(W/L)}$ ratio = _____ times $NMOS_{(W/L)}$ ratio in CMOS inverter.

(iii) Compare to BiCMOS logic family, CMOS logic family have _____ power dissipation and _____ speed of operation.

(iv) Programmable logic devices (PLDs) are fabricated with _____ at the cross points.

(vi) Among static NAND, dynamic NAND and domino logic NAND, ____ has higher device count.

(c) Draw NMOS NAND gate and NOR gate with **two** inputs. **6**

5 (a) Why CMOS is preferred over BJT in VLSI design? **3**

(b) Compare CMOS and Bi CMOS inverter with diagram. **6**

(c) Draw and explain dynamic shift register with load transistor clocking. **6**

OR

5 (a) State merits and demerits of CMOS logic family. **4**

(b) With diagram discuss organization semiconductor memory. **5**

(c) Draw and explain dynamic RAM cell. **6**

6	(a)	State the limitations of standard cell approach in VLSI design. How these limitations overcome in gate array approach?	**5**
	(b)	With flow diagram discuss steps of VLSI circuit design.	**5**
	(c)	Using ROM structure implement full adder circuit. Use transistor ROM structure for realization. Show logic function and truth table for implementation.	**5**

OR

6	(a)	Draw and explain BiCMOS NAND gate.	**5**
	(b)	What is the significance of gate array approach in VLSI design? Explain CMOS gate array with example diagram.	**5**
	(c)	Write short note on programmable logic array.	**5**